IN THE SPECIFICATION

Please replace the paragraph beginning on line 16 of page 5 with the following:

FIG. 1 is a block diagram of an adaptive PLL 100 according to embodiments of the present invention. Phase/frequency detector (PFD) 101 receives a signal REF 114 from reference oscillator 106 and an output Vo 107 from voltage-controlled oscillator (VCO) 105. PFD 101 generates two output signals, UP 110 and DN 111. UP 110 is a lead phase error signal which is a logic one during a cycle ~~of~~ if the phase of REF 114 leads Vo 107 and DN 111 is a lag error signal which is a logic one during a cycle if the phase of REF 114 lags Vo 107. UP 110 and DN 111 are used as up/down count inputs to Phase Polarity counter (PPC) 102 ~~as~~ that inputs to charge pump CP 104. PPC 102 has counter circuits that count REF 114 and generate two signals, Reset Delta 112 and Reset Total 113, which are used in Pump Counter (PC) 103 to generate a variable current Ipump 108. Charge-Pump (CP) 104 receives Ipump 108, UP 110, and DN 111 and generates the control voltage Vc 109 that sets the frequency of output Vo 107. The generation of a variable charge pump current Ipump 108 which is in turn used in a charge-pump circuit 104 to produce a control voltage Vc 109 for VCO 105 is one embodiment of the present invention. The control of variable current Ipump 108 and thus the response of Vc 109 to the dynamic phase and frequency differences in Vo 107 and REF 114 is another embodiment of the present invention and will be further explained in the following detailed description.

Please replace the paragraph beginning on line 9 of page 6 with the following:

The PLL 100 system in FIG. 1 first generates lead and lag phase error signals UP 110 and DN 111, respectively. The lead and lag phase error signals are used to generate a phase error signal input to PPC 102 which is proportional to the relative difference between the number of cycles during which REF 114 leads Vo 107 and the number of cycles during which REF 114 lags Vo 107. The phase error signal is increased when the lead error signal is present and decreased when the lag error signal is present (only one is present during a cycle). The absolute value of this phase error signal is compared to a threshold value. Likewise, each cycle of REF 114 is used to generate a time window

(corresponding to a number of cycles of REF 114). If the absolute value of the phase error signal reaches its threshold value before the time window is reached, then a first variable gain signal is increased. If the absolute value of the phase error signal fails to reach the threshold in the time window, then the first variable gain signal is decreased. A current, Ipump 108, is generated by multiplying a first reference current by the first variable gain and adding it to a second reference current. The first variable gain is limited to a value between a predetermined maximum and a predetermined minimum value. A second variable gain signal (SVG) is generated from the lead and lag error signals UP 110 and DN 111, respectively. When UP 110 is a logic one, SVG has a value of $+K$ and when the DN 111 is a logic one, SVG has a value of $-K$. Embodiments of the present invention use $K=1$. SVG multiplies Ipump 108 to generate a modified pump current (MPC) in charge pump CP 104. MPC is processed in CP 104 to generate Vc 109. In embodiments of the present invention, Vc 109 is generated by multiplying MPC by a first constant and adding it to the integral of MPC multiplied by a second constant. Vc 109 is then applied as the voltage control that sets the frequency of the output of VCO 105 that generates Vo 107. Vo 107 is compared to the REF 114 in the PFD 101 thus closing the feedback loop of PLL 100.

Please replace the paragraph beginning on line 16 of page 9 with the following:

FIG. 3 is a charge pump circuit according to embodiments of the present invention which accepts the variable current Ipump 108 and generates control voltage Vc 109 used to control the frequency of output Vo 107. Charge pump 104 receives signals UP ~~112~~ 110 and DN ~~113~~ 111 in the "time sum" (TS) circuit 301 and generates output TS 306. TS 306 has a value of plus one for the duration that UP 112 is a logic one and a value of minus one for the duration that DN 113 is a logic one. TS 306 is multiplied by Ipump 108 in multiplier 302 and generates output 308. Output 308 is multiplied by gain 304 (G1) and generates a voltage V1 309 equal to G1 times output 308. Output 308 is also multiplied by gain 303 (G2) and integrated by integrator 305 producing voltage V2 310. V1 309 and V2 310 are added in Sum 307 to produce control voltage Vc 109.

Control voltage Vc 109 controls VCO 105 and determines the frequency of the output Vo 107.

Please replace the paragraph beginning on line 1 of page 11 with the following:

FIG. 7 is a high level functional block diagram of a representative data processing system 700 suitable for practicing the principles of the present invention. Data processing system 700, includes a central processing system (CPU) 710 operating in conjunction with a system bus 712. System bus 712 operates in accordance with a standard bus protocol, such that as the ISA protocol, compatible with CPU 710. CPU 710 operates in conjunction with electronically erasable programmable read-only memory (EEPROM) 716 and random access memory (RAM) 714. Among other things, EEPROM 716 supports storage the Basic Input Output System (BIOS) data and recovery code. RAM 714 includes, DRAM (Dynamic Random Access Memory) system memory and SRAM (Static Random Access Memory) external cache. I/O Adapter 718 allows for an interconnection between the devices on system bus 712 and external peripherals, such as mass storage devices (e.g., a hard drive, floppy drive or CD/ROM drive), or a printer 740. A peripheral device 720 is, for example, coupled to a peripheral control interface (PCI) bus, and I/O adapter 718 therefore may be a PCI bus bridge. User interface adapter 722 couples various user input devices, such as a keyboard 724, mouse 726, touch pad 732 or speaker 728 to the processing devices on bus 712. Display ~~739~~ 738 which may be, for example, a cathode ray tube (CRT), liquid crystal display (LCD) or similar conventional display units. Display adapter 736 may include, among other things, a conventional display controller and frame buffer memory. Data processing system 700 may be selectively coupled to a computer or telecommunications network 741 through communications adapter 734. Communications adapter 734 may include, for example, a modem for connection to a telecom network and/or hardware and software for connecting to a computer network such as a local area network (LAN) or a wide area network (WAN). CPU 710 and other components of data processing system 700 may contain a PLL loop for generating clocks according to embodiments of the present invention.